teguh hofstee

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I am an independent researcher looking for a position as a research engineer. I am especially interested in leveraging compute for enabling interactive tools and interfaces even when faced with large amounts of data.

education

Stanford University / M.S. / Computer Science

June 2022 / Stanford, CA / Advisors: Pat Hanrahan, Mark Horowitz

I left after passing my Ph.D. qualifying exams to pursue research more aligned with my interests. I did my qualifying exams on modern hardware and software approaches for building Bounding Volume Hierarchies. https://hofstee.github.io/qual/

Carnegie Mellon University / B.S. / Electrical and Computer Engineering

August 2014 – May 2018 / Pittsburgh, PA / Advisor: Kayvon Fatahalian

Minor in Photography

experience

Independent Research Projects

Literature Mapping / I am building an interactive application to facilitate organization and discovery of large knowledge graphs (e.g. research papers). To enable visualization and interactive layout I am leveraging GPU-driven rendering and compute shaders. **Swift / Metal**

Algorithmic Visualization / I am interested in using visualization to explain concepts underlying GPU and other parallel algorithms to gain a high-level understanding and demystify the clever magic hidden and often overlooked in their details. **Rust / CUDA / TypeScript**

Stanford University / Ph.D. Candidate / Computer Science

September 2018 – June 2022 / Stanford, CA / Advisors: Pat Hanrahan, Mark Horowitz

My research was centered on computer architecture and high-performance systems. I worked on tools to make creating and debugging custom hardware easier, as well as improving hardware design languages.

Agile Hardware (AHA) Project / Played a key role in coordinating and integrating over 20 projects across multiple teams, including developing build and testing infrastructure for CGRA generation and application development, as well as conducting end-to-end system integration tests. Additionally, performed gate-level power analysis of the generated CGRA and contributed to the system architecture design of the SoC integrating the CGRA. **Python / C / C++ / SystemVerilog / misc. research languages + tools**

Stanford University / Undergraduate Research Assistant

June 2017 – August 2017 / Stanford, CA / Advisor: Pat Hanrahan

Extended Rigel (a domain-specific language for image processing) to allow for a more concise and readable notation for structuring image processing pipelines and applications which are automatically mapped down to efficient hardware designs to be synthesized on FPGAs. **Lua / SystemVerilog**

Carnegie Mellon University / Undergraduate Research Assistant

May 2016 – August 2016 / Pittsburgh, PA / Advisor: Kayvon Fatahalian

Helped create a high-performance research game engine targeting Vulkan, in conjunction with a modular shading system (which eventually became Slang), to reduce performance bottlenecks common in modern industrial game engines with new APIs such as D3D12 and Vulkan. **C++ / Vulkan**

IBM / Research Intern

June 2015 – August 2015 / Austin, TX

Architected, developed, and verified a streaming sorting accelerator using a Xilinx KU115 FPGA card on a POWER8 server. **C++ / SystemVerilog**

publications

Creating an Agile Hardware Design Flow

Stanford University AHA Agile Hardware Project / Design Automation Conference / 2020

Proposed a systematic approach (utilizing domain-specific languages and hardware generators) for designing and evolving high-performance and energy-efficient hardware-software systems for any application domain.

Shader Components: Modular and High Performance Shader Development

Yong He, Theresa Foley, Teguh Hofstee, Haomin Long, Kayvon Fatahalian / ACM Trans. Graphics / 2017

Proposed a higher-level abstraction to modern shading languages that allows for efficient organization of shader modules, so high-performance game engines can efficiently group shaders and perform fewer state changes while maintaining a desirable modular shader code structure. http://graphics.cs.cmu.edu/projects/shadercomp/

teaching

Stanford / CA / Parallel Computing (CS 149) / Fall 2021
CMU / TA / Parallel Computer Architecture and Programming (15-418) / Spring 2018